Bergquist
Thermal Clad®

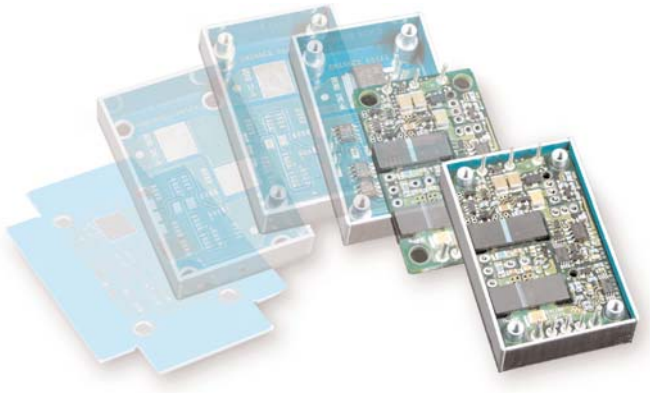
White Paper

TOOLS FOR AN OPTIMAL DESIGN

Things To Consider When Designing Circuits

Many factors come into play in circuit design with respect to etching, surface finishing and mechanical fabrication processes; such as holes, flatness, singulation and tolerances.

Fabrication of Thermal Clad is similar to traditional FR-4 circuit boards with regard to imaging and wet processing operations. However, secondary mechanical operations are unique, so the consideration of specific design recommendations are critical to ensure the manufacture of reliable, cost effective T-Clad circuits. This white paper will address design recommendations for circuit image, soldermask, legend and mechanical fabrication. Additional consideration for trace widths, spacing and clearances may be required for electrical integrity based on application voltage.



Cost Effective Basic Materials For An Optimal Design

Ideas For Minimizing Cost

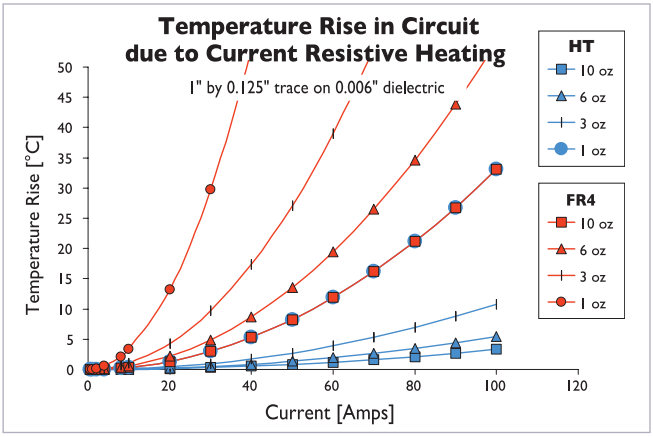
Material Stack Up - 5052 aluminum is our most cost effective offering. 6061-T6 aluminum is also available for applications which utilize the aluminum as a base for retaining fasteners or when considering specific fabrication applications.

Material Thickness - Using standard gauges will help control cost. Standard aluminum thicknesses are 1.0mm (0.040") and 1.6mm (0.062") and standard copper is 1.0mm (0.040"). Other thicknesses are also available.

Dielectric - The majority of applications are able to utilize our MP (multi-purpose) dielectric. If your application requires higher thermal performance or dielectric strength, please reference our characteristics of dielectric summary within our T-Clad Selection Guide.

Copper Circuit Foil - The thinner the circuit foil chosen, the lower the cost. It is common for customers to realize a 40% increase in current carrying capability as compared to FR-4 (see Figure 1). Copper thickness can often be reduced by using T-Clad.

Figure 1



Checklist To Optimal Design

Acceptable File Types For Design Submission

1. Preferred data format Gerber RS274X – include all layers (with embedded aperture list). DXF and some other formats are acceptable but take time to convert to Gerber and may become corrupted in the conversion process.
2. Provide mechanical print with part and array dimensions (if applicable), identify material, soldermask type and color and surface finish.
3. Identify areas of possible design violation.
4. Include operating voltage and maximum operating temperature.
5. Include engineering or circuit design contact information.

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For Additional Info (800) 347-4572
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Circuit Design

Material Utilization

Independent of the fabrication method chosen, square or rectangular designs will utilize the material most efficiently. The usable area of an 457 x 610mm (18.0" x 24.0") panel is 432 x 584mm (17.0" x 23.0") and a 508 x 610mm (20.0" x 24.0") is 483 x 584mm (19.0" x 23.0"). For best cost value, maximize use of this usable area. The shape of the part effects cost, so please reference the section on part singulation for helpful guidelines.

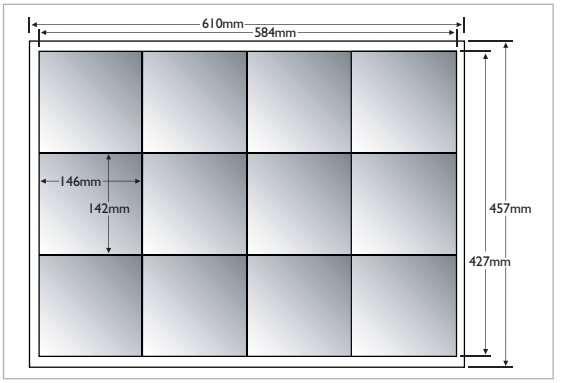
Surface Finish

- Green is the most commonly used soldermask color in the industry, and as a result it is the most cost effective. Other colors such as black, white, red and blue are also available.
- If possible, try to include legend (nomenclature) in the soldermask design. If not possible, consider white costs less than black.
- Regarding solder pad finish, HASL and Pb-free HASL are the most cost effective finishes. Other surface finishes such as ENIG, Ag, NiPdAu (for gold wire bond surfaces), and OSP (in panel and array form only) are available.

Base Plate Finish

- When using aluminum, a brushed finish is typical. Other finishes like anodize and irridite are available for additional cost. With copper, a brushed finish is also typical but may oxidize from handling and atmospheric conditions. Other finishes like nickel are available to prevent oxidation but will drive cost up.
- **When considering finishing the part edge and/or through hole edge, please note that an unfinished edge is more economical.**

Figure 2: Layout For Effective Use Of Space



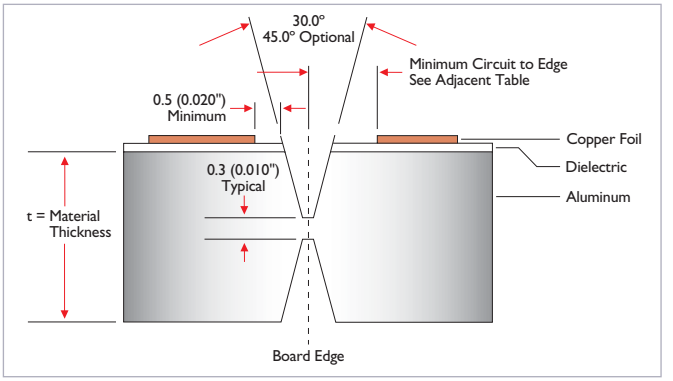
Part size is an important consideration in cost control. In Figure 2, part size is 146 x 142mm (5.75" x 5.59") and panel utilization is 90%. This high utilization was achieved by reducing part size from the original 146 x 145mm (5.75" x 5.71") - only a 3mm change. The result is an increase in parts per panel from 8 to 12 utilizing the same amount of material (30% gain in panel utilization).

Part Fabrication

V-Scoring

V-scoring is a viable process selection for both low and high volume production because it allows for maximum material utilization. V-scoring is also a preferred process for prototypes with rectangular geometries having the benefit of no tooling costs. Holes can be drilled or punched prior to scoring. Typical tolerance for part size, hole position to part edge, and circuit to edge is +/- 0.25mm (0.010"). V-scoring is a great alternative for arrays. Circuit to edge spacing can be reduced over a typical blanked part (see Section 1.4 on page 4 of this document).

Figure 3: V-Scoring Guidelines



Hole Piercing / Perimeter Blanking

Hole piercing and perimeter blanking are some of the most cost effective processes for moderate to high volume applications. Blank tooling can accommodate complex part geometries and can be held to a very tight tolerance. In addition to blanking the part perimeter, piercing patterns of internal holes can be produced with the most accuracy and the greatest degree of repeatability. However, T-Clad that is to be blanked in production should be considered as early in the design process as possible. Part design is critical to ensure blanking feasibility as there are specific guidelines to be considered. Each design should be evaluated to the recommendations defined in this document prior to beginning the tool planning process.

Figure 3: Circuit to Edge Distance

Material Thickness (t)	Minimum Circuit to Edge
1.0 mm (0.040")	0.66 mm (0.026")
1.6 mm (0.062")	0.74 mm (0.029")
2.0 mm (0.080")	0.79 mm (0.031")
3.2 mm (0.125")	0.94 mm (0.037")

Part Fabrication

Milling / Drilling

Milling/drilling processes are typically used for prototype or low volume production with complex geometries. These processes are typically not cost effective for moderate to high volume applications.

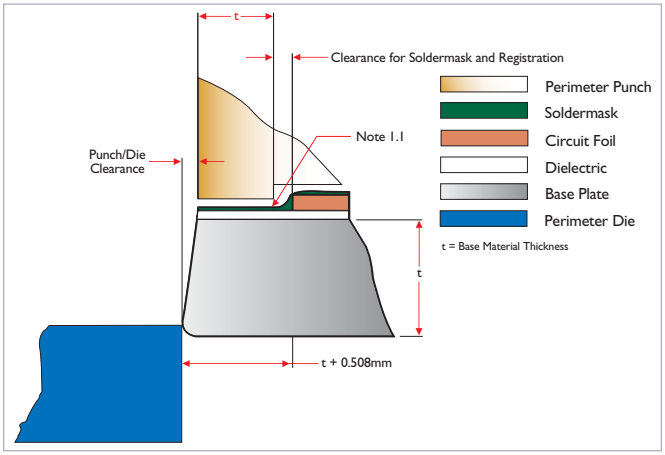
Circuit to Edge

When planning to blank a part perimeter, the distance between the circuit pattern and the part edge is critical. To allow for sufficient relief for the circuitry (See Figure 4), the standard minimum distance from circuit to part edge is one material thickness plus 0.5mm (0.020"). If the circuit foil is 2oz or higher, the face of the perimeter punch must be designed to allow for uniform support around the part perimeter.

Active circuitry that needs to be isolated from the base plate should be placed a minimum of one material thickness plus 0.5mm (0.020") from the edge of the hole. If the circuit is a ground pattern, or same potential as the base plate, then the circuitry may go closer. Standard practice is to always leave a 1.3mm (0.005") relief around a pierced hole.

Note: The minimum diameter we can pierce is equivalent to one material thickness. Higher voltages may require greater clearances.

Figure 4: Punch to Die Clearance



Radii on Corners

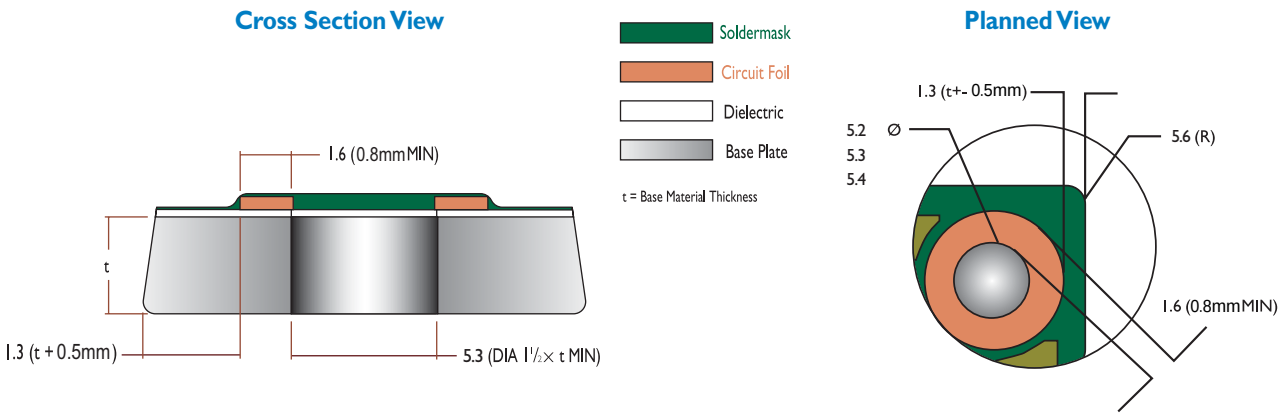
Punching requires that all inside and outside corners be designed with a minimum radius. It is recommended that one material thickness minimum radius be on all corners. When desired, it is possible to go down to one half material thickness radius however, this requires special tooling costs.

Flatness

Part design, as well as the manufacturing process, affects flatness of an Insulated Metal Substrate (IMS®) board. There is also an effect from the differential coefficient of thermal expansion (CTE) between the circuit and the base layer. That effect is determined by the base plate material selection and ratio of copper foil to base plate thickness.

For IMS®, panel or part, there is always the potential for some bow caused by the difference in CTE between the circuit layer and the base plate. Flatness can be further optimized by using copper base metal instead of aluminum and with proper overall design. Generally, if the thickness of the copper layer is less than 10% of the substrate thickness, the aluminum will be mechanically dominant. Constructions with more circuit copper than 10% of the substrate thickness can exhibit a bow. Copper foil thicknesses less than 10% of the base plate thickness can be controlled well within IPC specifications. Flatness can be further optimized with proper tool design.

Figure 5: Hole and Circuit to Edge Clearance



Note: Use of a soldermask is recommended.

Bold numbers within these drawings reference table on pages 4-5 of this document.

DESIGN CATEGORY	DESIGN PARAMETER	STANDARD DESIGN RECOMMENDATION AND SPECIFICATION	
1.0 Circuit Design	**1.1** Minimum Circuit Width	**Circuit Thickness**	**Minimum Line Width**
		35µm (1 oz)	0.13mm (0.005")
		70µm (2 oz)	0.15mm (0.006")
		105µm (3 oz)	0.18mm (0.007")
		140µm (4 oz)	0.20mm (0.008")
		210µm (6 oz)	0.15mm (0.010")
		280µm (8 oz)	0.38mm (0.015")
		350µm (10 oz)	0.38mm (0.015")
	1.2 Minimum Space and Gap Single Layer	**Single-Layer (non-plated)**	**Multi-Layer (plated)**
		35µm (1 oz) - 0.18mm (0.007")	35µm (1 oz) - 0.23mm (0.009")
		70µm (2 oz) - 0.23mm (0.009")	70µm (2 oz) - 0.28mm (0.011")
		105µm (3 oz) - 0.30mm (0.012")	105µm (3 oz) - 0.36mm (0.014")
		140µm (4 oz) - 0.36mm (0.014")	140µm (4 oz) - 0.41mm (0.016")
		210µm (6 oz) - 0.51mm (0.020")	210µm (6 oz) - 0.56mm (0.022")
		280µm (8 oz) - 0.61mm (0.024")	280µm (8 oz) - 0.66mm (0.026")
		350µm (10 oz) - 0.76mm (0.030")	350µm (10 oz) - 0.81mm (0.032")
	1.3 Minimum Circuit to Edge Blanking	One material thickness	
	1.4 Minimum Circuit to Edge v - scored/milled/routed	**Material Thickness**	**Circuit to Edge Distance**
		1.0mm (0.040")	0.66mm (0.026")
		1.6mm (0.062")	0.74mm (0.029")
		2.0mm (0.080")	0.79mm (0.031")
		3.2mm (0.125")	0.94mm (0.037")
	1.5 Minimum Conductor to Hole Edge	One material thickness	
	1.6 Copper Land w/ Non-Plated Through Holes	Purchased non-plated through hole is 0.76mm (0.030") minimum	
	1.7 Minimum Character Height for Etched Nomenclature	1.5mm (0.060")	
2.0 Soldermask Design	**2.1** Minimum Soldermask Line Width	0.20mm (0.008")	
	2.2 Soldermask Pad Apertures	Bergquist recommends that whenever possible, design the soldermask overlap on top of 0.25mm (0.010") copper foil	
	2.3 Minimum Soldermask Aperture Size	0.20mm x 0.20mm (0.008" x 0.008")	
	2.4 Minimum Character Height & Line Width for Nomenclature	0.20mm x 0.20mm (0.008" x 0.008")	
	2.5 Soldermask Color	Green is standard (other colors available)	
	2.6 Character Height/Width (In Soldermask)	Minimum character height / Minimum line width 0.010"	
3.0 Legend Design	**3.1** Nomenclature to Pad (Ink Jet Printing)	Recommended minimum distance from nomenclature feature to nearest pad is 0.25mm (0.010")	
	3.2 Character Height / Width	1.5mm (0.060") minimum height, 0.15mm (0.006") minimum width	
	3.3 Minimum Distance to Board Edge	One material thickness	
	3.4 Nomenclature Color	White is standard (black optional)	
4.0 Surface Finish	**4.1** Surface Finish Available	HASL, Lead Free HASL, (EPIG), ENIG, OSP (Intel CU56)	
5.0 Mechanical Design	**5.1** Hole to Board Edge	Minimum distance from edge of hole to edge of board is one material thickness	
	5.2 Punched Hole Size	Minimum punched hole size is 1.5x material thickness	
	5.3 Minimum Drilled Hole Diameter - Copper Base Plate	One material thickness	
	5.4 Minimum Drilled Hole Diameter - Aluminum Base Plate	**Material Thickness**	**Drilled Hole Diameter**
		1.0mm (0.040")	0.76mm (0.030")
		1.6mm (0.062")	0.76mm (0.030")
		2.0mm (0.080")	1.0mm (0.040")
		3.2mm" (0.125)	1.6mm (0.062")
	5.5 Minimum Drilled via Diameter for Circuit Layer	0.36mm (0.014")	
	5.6 Minimum Edge Radius	One material thickness for blanking, no radius for V-scoring	
	5.7 Minimum Circuit to Edge for Blanking	One material thickness plus 0.51mm (0.020")	

TOLERANCES
IPC-6012 35.1 80%
IPC-6012 35.1 80%
IPC-6012 35.1 80%
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IPC-6012 35.2 20%
IPC-6012 35.2 20%
+/- 0.25mm (+/-0.010")
+/- 0.25mm (+/-0.010")
+/- 0.25mm (+/-0.010")
+/- 0.25mm (+/-0.010")
+/- 0.14mm (+/-0.005")
+/- 0.25mm (+/-0.010")
+/- 0.25mm (+/-0.010")
+/- 0.25mm (+/-0.010")
+/- 0.05mm (+/-0.002")
+/- 0.05mm (+/-0.002")
+/- 0.05mm (+/-0.002")
+/- 0.05mm (+/-0.002")
+/- 0.13mm (+/-0.005")

The shaded blue areas represent Bergquist circuit processing capabilities. If your application requires different specifications, please contact Bergquist Sales.

Guideline 1.3: The minimum circuit to edge blanking distance allows the punch to engage the metal baseplate and dielectric without damaging adjacent circuitry.

Guideline 1.4: The minimum distance from circuit to edge must be met to provide isolation from the circuitry to the baseplate. Note: Additional distance from circuit to hole may be required depending on application and proof testing requirements.

Guideline 1.5: The minimum conductor to hole edge distance must be achieved to provide isolation from circuitry to the base.

Guideline 1.7: The minimum character height for etched nomenclature must be met for optimum legibility.

Guideline 2.1: Minimum soldermask line width is needed for proper adhesion of the soldermask to the board surface. This is also an important consideration for maintaining separation between pads (solderdams).

Guideline 2.2: Solder pad apertures designed with overlap ensure proper adhesion of the soldermask to the board surface and prevention of exposure to copper and bridging between features.

Guideline 2.3: The minimum soldermask specification keeps the pads exposed so they can accept the surface plating and ensures the pad will remain large enough to be functional.

Guideline 2.4: A standard minimum character height and width is set to ensure legibility.

Guideline 3.1: A character width and height are specified for silk screening to assure legibility and adhesion.

Guideline 3.2: The minimum distance from silk screen to the nearest pad is required for registration to keep the legend ink off of solderable surfaces.

Guideline 3.4: A minimum distance to board edge is specified to ensure clearance for punch land, for registration purposes and to maintain legibility.

Guideline 5.1: The minimum distance from hole edge to board edge is important to avoid material distortion during processing.

Guideline 5.2: A minimum punched hole size is recommended to ensure tool strength integrity during processing and to avoid premature tool wear.

Guidelines 5.3: A minimum drilled hole diameter for the copper base plate is in place to ensure tool strength integrity during processing and to avoid premature tool wear.

Guidelines 5.4: The aluminum base plate has a minimum drilled hole diameter specification to ensure tool strength integrity during processing and to avoid premature tool wear.

Guideline 5.5: The circuit layer's recommended minimum drilled via diameter ensures tool strength integrity during processing and helps to avoid premature tool wear.

Guideline 5.7: The minimum circuit to edge blanking distance allows the punch to engage the metal base plate and dielectric without damaging adjacent circuitry and improves tool life.

Testing Options

Electrical Opens and Shorts

Verification can be done with two methods.

1. For single-layer boards using A.O.I. (Automatic Optical Inspection) is the most cost-effective method. Using original Gerber data to compare to the etch panel will find any anomalies, even in an etch-down condition.
2. The more traditional "Bed-of-Nails" testing is also available. This requires a fixture charge and is a higher cost method. It is the only viable method for two-layer constructions.

Proof Testing or (HiPot)

Testing is done to verify dielectric strength integrity of a T-Clad board.

1. Proof testing done in panel form is the most cost effective method. This form of testing is done at post-etch condition, prior to surface finish or final fabrication.
2. The recommended method for safety agency requirements on T-Clad assemblies is an individual piece-part or array-part test. This method 100% tests and marks each finished board and/or array. This method requires a fixture charge.
3. When higher test voltages are required to meet safety agency requirements; standard clearances for fabrication may not be enough to allow for "Creepage Clearance" to meet test voltages. These minimum creepage distances can be found in safety agency standards or IPC-2221 for reference.

Advanced Process Technologies

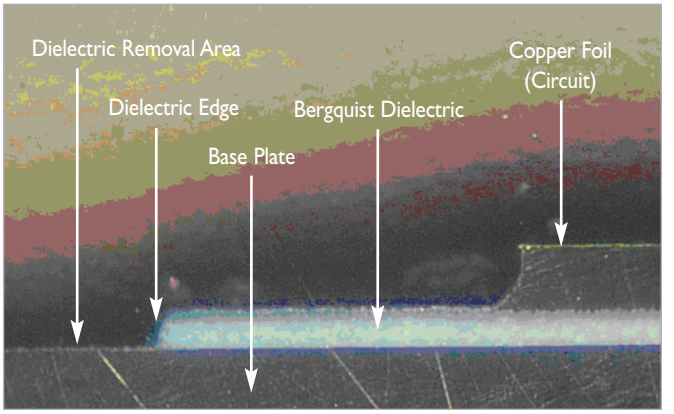
Part Forming

Thermal Clad is designed with a copper or aluminum base plate that can be formed. In order to maintain thermal and electrical integrity, circuits cannot go across the bent area.

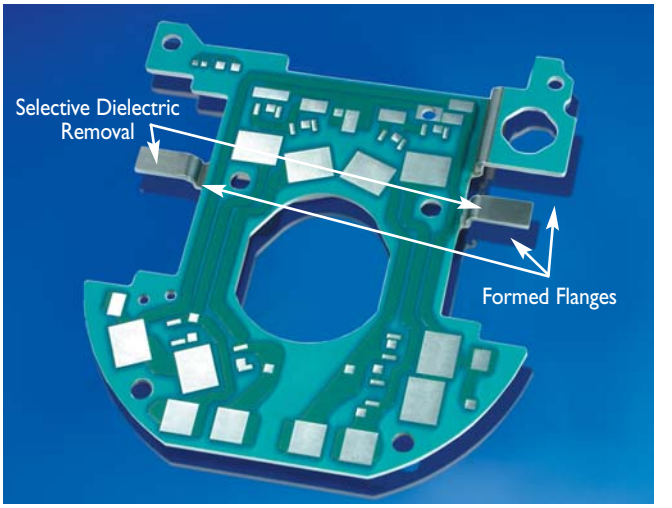
Selective Dielectric Removal

Bergquist has developed a secondary process for selectively removing dielectric to expose the base plate. This surface can be surface finished like the circuit pads. We are not limited to geometry or size of the dielectric removal area. Selective removal features can be placed very accurately with respect to the circuits. For more detail regarding design and tolerance recommendations, please contact your Bergquist representative.

Figure 6: Dielectric Removal



Figures 7: Dielectric Removal in Motor Control Application



Thermal Clad is a versatile substrate. In this motor control application, the dielectric has been selectively removed and the metal has been formed with three-dimensional features.

Two-Layer Design Considerations

Benefits and Considerations

T-Clad dielectrics in two-layer constructions have significant benefits in overall design when compared to two-layer FR-4 constructions. These benefits include; higher power density, electromagnetic shielding and/or improved capacitive coupling. While designing your two-layer circuit, please keep these items in mind:

- The inner-layer copper pattern is not considered a primary current carrying element, so it does not need to be thick copper. These constructions are usually a 70 micron (2 oz) foil plated-up maximum.
- Due to the lower thermal impedance of T-Clad dielectric as compared to FR-4, thermal via's are not usually required. Formulas can be provided to make these determinations.
- When using a copper base plate, connections from the circuits to the base plate are possible using a plated Blind-via.
- Using electrical/thermally conductive hole fill materials creates a flat surface area enabling mount pads for large devices and prevents solder voiding.
- A selective dielectric removal process can be used to expose to the inner-layer and/or the base plate for component attachment. This design reduces thermal resistance.

Material Selection and Fabrication

Two-layer designs incorporate additional amounts of copper and dielectric thickness over single-layer designs. As a result, additional considerations must be made with regard to material construction choices and fabrication.

- Flatness is affected by the amount of copper so CTE rules must be considered in the equation. Most heavy copper constructions will require a thicker aluminum base substrate or copper base to prevent bowing.
- The additional dielectric thickness will also create the need for larger minimum distances in drilling, scoring, routing and punching. See the section regarding fabrication.

Designing A Non-Rectangular Array

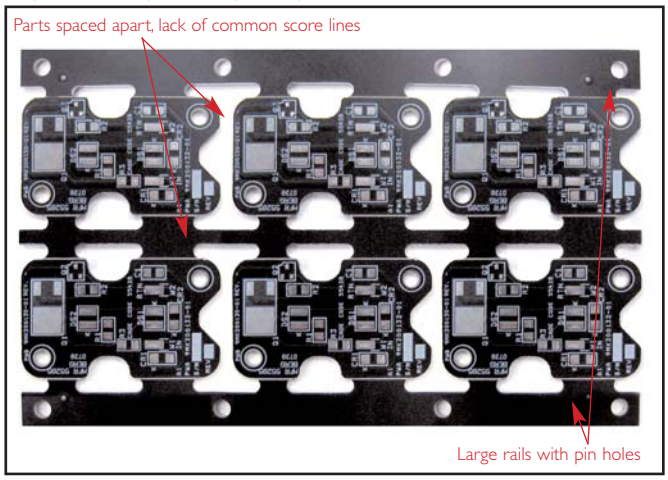
Comparing An Array In Three Different Considerations

- Non-rectangular designs typically require additional spacing in the array for milling or punching the shape. Often a combination of scoring and milling/punching is required to create the part shape and allow parts to be separated from the array after assembly. Additional process steps and reduced material utilization can impact cost.

Design Considerations For Better Material Utilization

- Are rails required for assembly? Rails consume material that will be discarded after parts are separated from the array. When designing an array, size and number of rails should be considered to optimize panel utilization. The reduced rail design in Figure 9 uses less material than Figure 8, and even less material is required for the design with no rails in Figure 10.

Figure 8: Original Array Design



- Will assembled components require parts to be spaced further apart? This can result in multiple score lines and reduced material utilization. Consider part orientation in the array. Alternating orientation may allow components to nest, maximizing material utilization. In Figure 8 parts are spaced further apart and use more material as compared to the common score lines used in Figures 9 and 10.

Figure 9: Improved Design

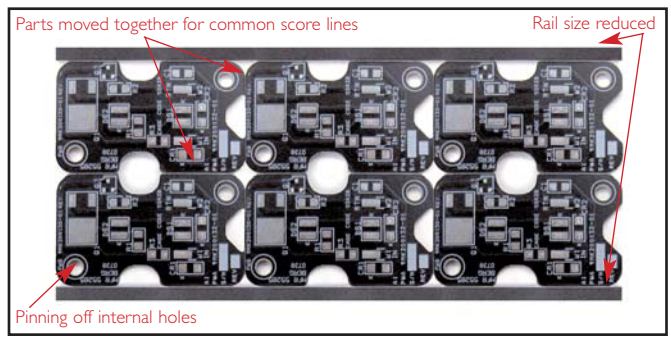
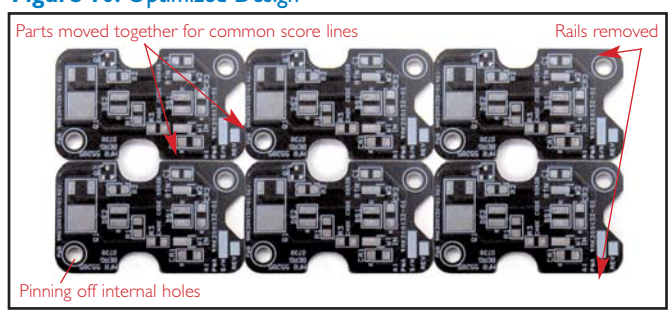


Figure 10: Optimized Design



THE BERGQUIST COMPANY

www.bergquistcompany.com

The Bergquist Company
North American Headquarters
18930 West 78th Street
Chanhassen, MN 55317
Phone: 800-347-4572
Fax: 952-835-4156

The Bergquist Company
European Headquarters
Bramenberg 9a, 3755 BT Eemnes
Netherlands
Phone: 31-35-5380684
Fax: 31-35-5380295

The Bergquist Company- Asia
Room 15, 8/F, Wah Wai Industrial
Centre No. 38-40
Au Pui Wan Street,
Ph: 886-2-2778-1048
Fax: 886-2-2778-1049

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